

	Type	Ref #	Hits	Search Text
1	BRS	S357	280	703/19.ccls.
2	BRS	S358	0	(circuit adj timing) same fanis
3	BRS	S359	0	(circuit adj timing) and fanis
4	BRS	S361	0	(circuit adj timing) same fanins
5	BRS	S360	51	(circuit adj timing) and fanins
6	BRS	S362	2292	(circuit adj timing) same delay\$
7	BRS	S363	0	((circuit adj timing) same delay\$) and (sort\$3 same fanins)
8	BRS	S364	0	((circuit adj timing) same delay\$) and (sort\$3 near fanins)
9	BRS	S365	2	(sort\$3 near fanins)
10	BRS	S366	14	(sort\$3 same fanins)
11	BRS	S367	12	(fanins).ti.
12	BRS	S368	8	(fanins).ti. and (circuit same delay)
13	BRS	S369	7	(fanins).ti. and (circuit same delay) and paths
14	BRS	S370	33	(first adj critical path) and (second adj critical adj path)
15	BRS	S371	10	(first adj critical path) and (second adj critical adj path) and (reduce same delay\$3)
16	BRS	S372	6	(first adj critical path) and (second adj critical adj path) and (reduce same delay\$3) and node
17	BRS	S373	2	"5648913".pn.

	Type	Ref #	Hits	Search Text
18	BRS	S374	1	"5648913".pn. and (timing same delays)

	DBs	Time Stamp	Comments	Error Definition
18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2006/07/27 16:21		

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2	INZZ	1 AND aplus.AS.	unrestricted	0	-
3	INZZ	1 AND circuit SAME delay	unrestricted	2	show titles
4	INZZ	Xu-S.AU.	unrestricted	309	show titles
5	INZZ	4 AND timing	unrestricted	2	show titles
6	INZZ	(aplus ADJ design ADJ technology).AS.	unrestricted	0	-

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1. **Synthesis for high-density and high-performance FPGAs**
by Xu, Songjie, Ph.D., University of California, Los Angeles, 2000, 213 pages; AAT 3058483

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2	BRS	L17	1450	716/6.ccls.	US- PGPUB; USPAT; USOCR; EPO; JPO; DERWEN T; IBM_TDB	2006/07/27 18:23